REMARKS

Applicants wish to thank the Examiner for participating in the case interview. The Examiner and the Applicants' representative discussed claim modifications that could possibly result in allowance of the claims. As indicated on the Examiner Summary form, no agreement was reached as to the specific content of any claims. Applicants have amended the claims herein.

In accordance with the foregoing, claims 1, 3, 6, 29 and 31 have been amended. Claims 1-6 and 9-31 are pending and under consideration. In the above-identified Office Action, the Examiner has objected to the specification due to what was a minor editorial problem in the first paragraph beginning on the last page of page 31 and continuing on page 32. Applicants replaced this paragraph in Applicants' amendment dated July 28, 2004, as suggested by the Examiner (changed "Fig. 4" to "Fig. 23" on page 32 of the specification). Applicants respectfully request that the objection be withdrawn.

Claims 1, 6, 9 and 29 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Pat. No. 5,612,963 (Koenemann) in view of an article by Jas, entitled "Hybrid BIST Based on Weighted Pseudo-Random Testing: a New Test Resource Partitioning Scheme" (Jas).

According to Koenemann, it teaches a random pattern method and system of providing test signals to circuits on an integrated computer circuit chip. The system of Koenemann includes a means for generating a pseudo-random signal sequence, a weighting means for receiving the pseudo-random sequence and for producing a weighted output sequence, and a weight storage means for storing a sequence of two bit weights. According to Koenemann, the system requires only one connection to a linear feedback shift register device. *See* Koenemann, column 3, lines 4-13.

According to Jas, it presents a test resource partitioning scheme that is a hybrid approach between external testing and Built-in Selft-test. The scheme in Jas reduces tester storage requirements and tester bandwidth requirements in comparison to conventional external testing and requires less area overhead than a full BIST implementation providing the same fault coverage. The approach in Jas is based on weighted pseudo-random testing. *See* Jas, Abstract.

According to the present invention, it shortens testing time of an integrated circuit and solves problems of the Deterministic Stored-Pattern Testing (DSPT) and the Built-in Self Test (BIST) approaches to testing. In particular, the problems related to BIST are solved by a method

of interpolating a pseudo random pattern with an ATPG pattern and using the result. *See* Specification, page 21, lines 9-15. More specifically, as test patterns generated by the pattern generator built into the integrated circuit are modified by the pattern modifier and inputted to the shift registers, the number of scan paths inputted to the shift registers is increased. As a result, the number of stages of the scan path can be decreased, which allows the testing time of the integrated circuit to be largely shortened. *See* Specification, page 9, lines 5-12.

The interpolating feature is recited in the language of currently amended independent claims 1, 6, and 29, for example, as "interpolating said pseudo random patterns with said ATPG patterns." Applicants respectfully submit that the present invention, as defined by independent claims 1, 6 and 29, is not rendered obvious by Koenemann in view of Jas, as neither reference teaches or suggests interpolating pseudo random patterns with ATPG patterns, as in the present invention.

As the Examiner admits, Koeneman does not teach the generation of ATPG test patterns at all. *See* Office Action, at page 3, item 5. Rather, Koeneman merely teaches the generation of a pseudo-random signal sequence and a weighting means for receiving the pseudo-random sequence and producing a weighted output sequence. *See* Koeneman, column 3, lines 4-8. Thus, it follows that Koeneman cannot teach or suggest, "interpolating said pseudo random patterns with said ATPG patterns," as recited in the above-identified claims, as there are no ATPG patterns in Koeneman.

Likewise, Jas does not teach or suggest the above-quoted language of the claims. Rather, Jas teaches a hybrid BIST (a scheme involving combining external data from the tester along with BIST hardware on the chip to provide a hybrid test solution for a particular module or core) approach based on weighted pseudo-random testing. In the method of Jas, weight sets of a pseudo-random pattern are compressed and stored. *See* Jas, page 3, last paragraph. Although Jas provides that top-up deterministic test vectors applied from a tester to detect random pattern resistant faults are obtained by applying pseudo-random patterns using a STUMP architecture and then performing an ATPG for a group of remaining undetected faults, no information whatsoever is disclosed or suggested relating to the above-identified feature of the claims.

Therefore, in light of the foregoing, claims 1, 6 and 29 are patentable over Koenemann in view of Jas, as neither Koenemann nor Jas, taken alone, or in combination, teaches or suggests the feature identified by the above-quoted language of the claims. As claim 9 depends from claim 1, Applicants respectfully submit that claim 9 is patentable over the references for at least the reasons offered above with respect to claim 1, in addition to other reasons. For example,

neither of the references teaches or suggests selection of a combination of a pseudo random pattern and an ATPG pattern from generated pseudo random patterns.

Claims 11, 13, 15, 17, and 19 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Koenemann in view of Jas, and further in view of U.S. Pat. No. 6,708,305, to Farnsworth (Farnsworth). Farnsworth merely generates a pseudo random pattern and aligns the pattern with a particular scan cycle. As previously discussed, Koenemann and Jas do not teach the above-identified feature of the present invention. Farnsworth is completely silent as to interpolating pseudo random patterns with ATPG patterns, as in the present invention. Therefore, Applicants respectfully submit that claims 11, 13, 15, 17, and 19 are patentable over the references, as none of the references, taken alone or in combination, teach or suggest the features of the present invention as defined by claims 11, 13, 15, 17, and 19, via claim 1.

Claim 19 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Koenemann in view of Jas and further in view of U.S. Pat. No. 6327687 (Rajski). Applicants submit that Rajski does not teach or suggest the above-identified feature. Rajski merely teaches a method for compressing test patterns that are to be applied to scan chains in a test circuit. In Rajski, no information is disclosed or suggested regarding the above-identified feature of the present invention. Therefore, claim 19 is patentable over Koenemann in view of Jas and further in view of Rajski, none of the references teach or suggest the above-identified feature of claim 19 recited via claim 1.

Claims 21, 23, 25 and 27 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Koeneman in view of Jas, in view of Rajski, and further in view of U.S. Pat. No. 5,991,909 (Rajski 2). Rajski 2 discloses a parallel decompressor capable of concurrently generating in parallel multiple portions of a deterministic partially specified data vector. Although Rajski 2 discloses that the parallel decompressor can function as a PRPG for generating pseudo-random data vectors, Rajski 2 does not teach or suggest interpolating, as identified by the language of claims 21, 23, 25 and 27, via claim 1. Therefore, Applicants respectfully submit that claims 21, 23, 25 and 27 are patentable over the references, as none of the references, taken alone or in combination, teach or suggest the above-identified feature of the claims.

Claims 2, 4 and 30 have been rejected by the Examiner under 35 U.S.C. § 103(a) as being unpatentable over a paper issued to Carl Barnhart *et al.*, entitled, "OPMISR: The Foundation for Compressed ATPG Vectors" (hereinafter Barnhart). According to the present invention as recited in claims 2 and 30, a testing apparatus for an integrated circuit or the integrated circuit itself includes "an output verifier" that verifies output results from a masking function performed to convert an indeterminate value into a state value of "0" or "1" to mask the

indeterminate value.

Regarding independent claims 2 and 30, Applicants submit that these claims are patentable over Barnhart, as Barnhart does not teach or suggest an output verifier, as identified by the language of claims 2 and 30. Although Barnhart discloses information relating to mask logic, it does not disclose or suggest any information relating to a verifier. The reference on page 751 of Barnhart to verification refers to switching between a first configuration in which the MISR is configured as a signature generator that accumulates and compresses scan chain contents to a second configuration in which MISR feedbacks are disabled. In particular, Barnhart states that it must be verified that switching between the two configurations does not destroy the states of the scan cells. Thus, the verification in Barnhart is with regard to destroying states of the scan cells during switching of configurations and is not at all related to verifying results of a masking operation, as claimed in the present invention.

Therefore, claims 2 and 30 are patentable over Barnhart, as Barnhart does not teach or suggest an output verifier, as identified by the language of claims 2 and 30. As claim 4 depends from independent claim 2, it is also patentable over the reference for at least the reason offered above with respect to claim 2.

On page 10, the Examiner rejected claims 3, 5, 10 and 31 under 35 U.S.C. § 103(a) as being unpatentable over Koenemann in view of Jas, and further in view of Barnhart. Regarding independent claims 3 and 31, Applicants respectfully submit that these claims are patentable over the references, as none of the references, taken alone or in combination, teach or suggest interpolating as identified in the claims. Barnhart is not directed to generating test patterns and does not mention or suggest interpolating (see argument above regarding Koenemann and Jas).

In addition, Applicants submit that claims 3, 5, 10 and 31 are patentable over the references, as neither of the references, taken alone or in combination, teaches or suggests an output verifier, as identified by the language of claims 3 and 31. As claims 5 and 10 depend from independent claim 3, these claims are patentable over the references for at least the reasons offered with respect to independent claim 3.

Claims 12, 14, 16, and 18 have been rejected as being unpatentable over Koenemann in view of Jas. Applicants submit that claims 12, 14, 16 and 18 are patentable over Koenemann in view of Jas, as neither reference, taken alone or in combination, teaches or suggests interpolating, as identified in claim 3, from which claims 12, 14, 16, and 18 depend.

On page 12 of the Office Action, the Examiner rejected claim 20 under 35 U.S.C. § 103(a) as being unpatentable over Koenemann in view of Jas, in view of Barnhart, and further in view of Rajski. As previously argued, neither Koenemann, Jas, nor Barnhart teaches or

suggests interpolating as recited in claim 20 via claim 3. Applicants respectfully submit that Rajski also does not teach the interpolating of claim 20 via claim 3, as Rajski is directed to a method for compressing test patterns and is completely silent on interpolating.

Claims 22, 24, 26, and 28 were rejected under 35 U.S.C. § 103 (a) as being unpatentable over Koenemann, in view of Jas, in view of Barnhart, in view of Rajski, and in view of Rajski 2. Applicants respectfully submit that claims 22, 24, 26, and 28 are patentable over the references, as none of the references, taken alone or in combination, teach or suggest the interpolating identified in claim 3, from which claims 22, 24, 26, and 28 depend. Further, none of the references, taken alone or in combination, teach or suggest the output verifier identified in the language of claim 3.

It is respectfully submitted that all claims satisfy the requirements of 35 U.S.C. § 103. It is further submitted that the claims are not taught, disclosed or suggested by any of the references. The claims are therefore in a condition suitable for allowance. An early Notice of Allowance is requested.

If any further fees, other than and except for the issue fee, are necessary with respect to this paper, the USPTO is requested to obtain the same from deposit account number 19-3935.

If the Examiner has any remaining issues to be addressed, it is believed that prosecution can be expedited by the Examiner's contacting the undersigned attorney for a telephone interview to discuss resolution of such issues.

Respectfully submitted,

STAAS & HALSEY LLP

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By: _____
Reginald D. Lucas
Registration No. 46,883

1201 New York Avenue, NW, Suite 700
Washington, D.C. 20005
Telephone: (202) 434-1500
Facsimile: (202) 434-1501

S&H Form: (10/03)